SAMSUNG
Design Solution Partner

CoAsia SEMI Corporation

Chiplet Solution PKG platform trend and hedge

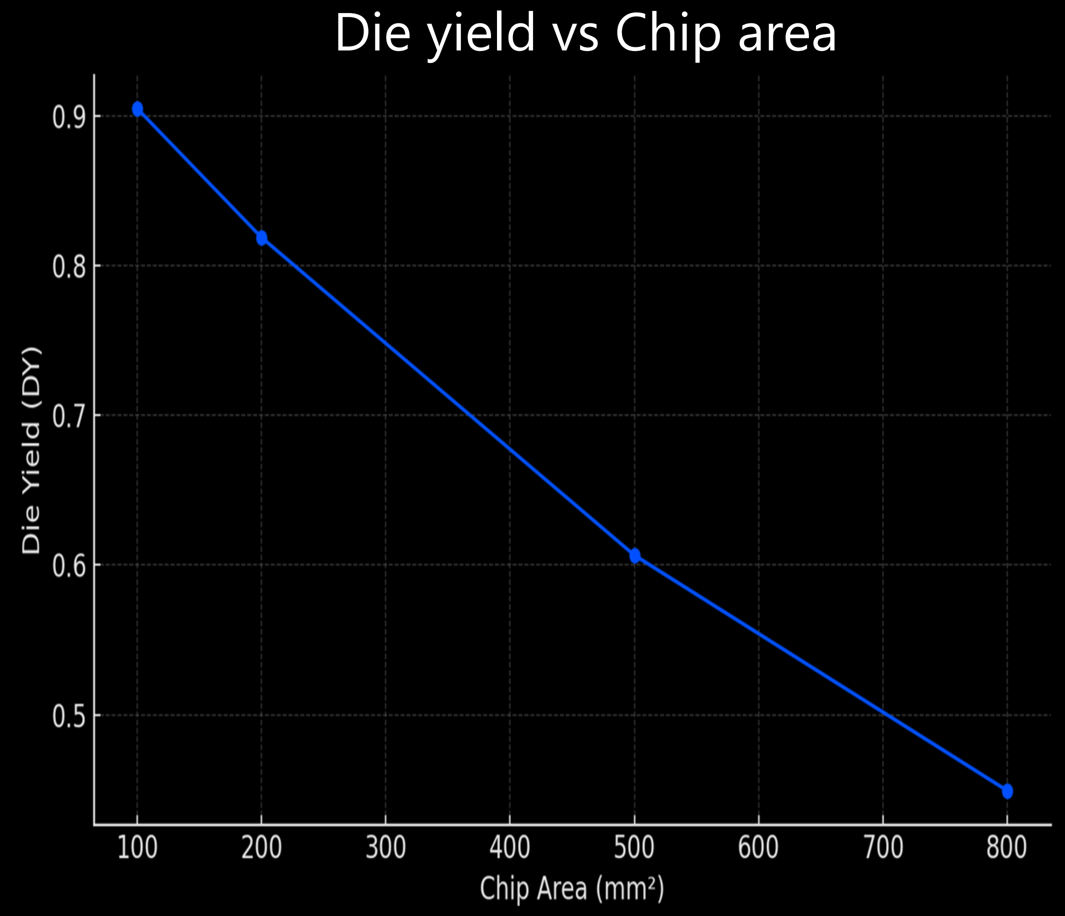
Why need Chiplet PKG solution?

- **Die size ≒ 1reticle size < yield 50% → How to design die for PPA by Chiplet?**

Die size trend

From AMD

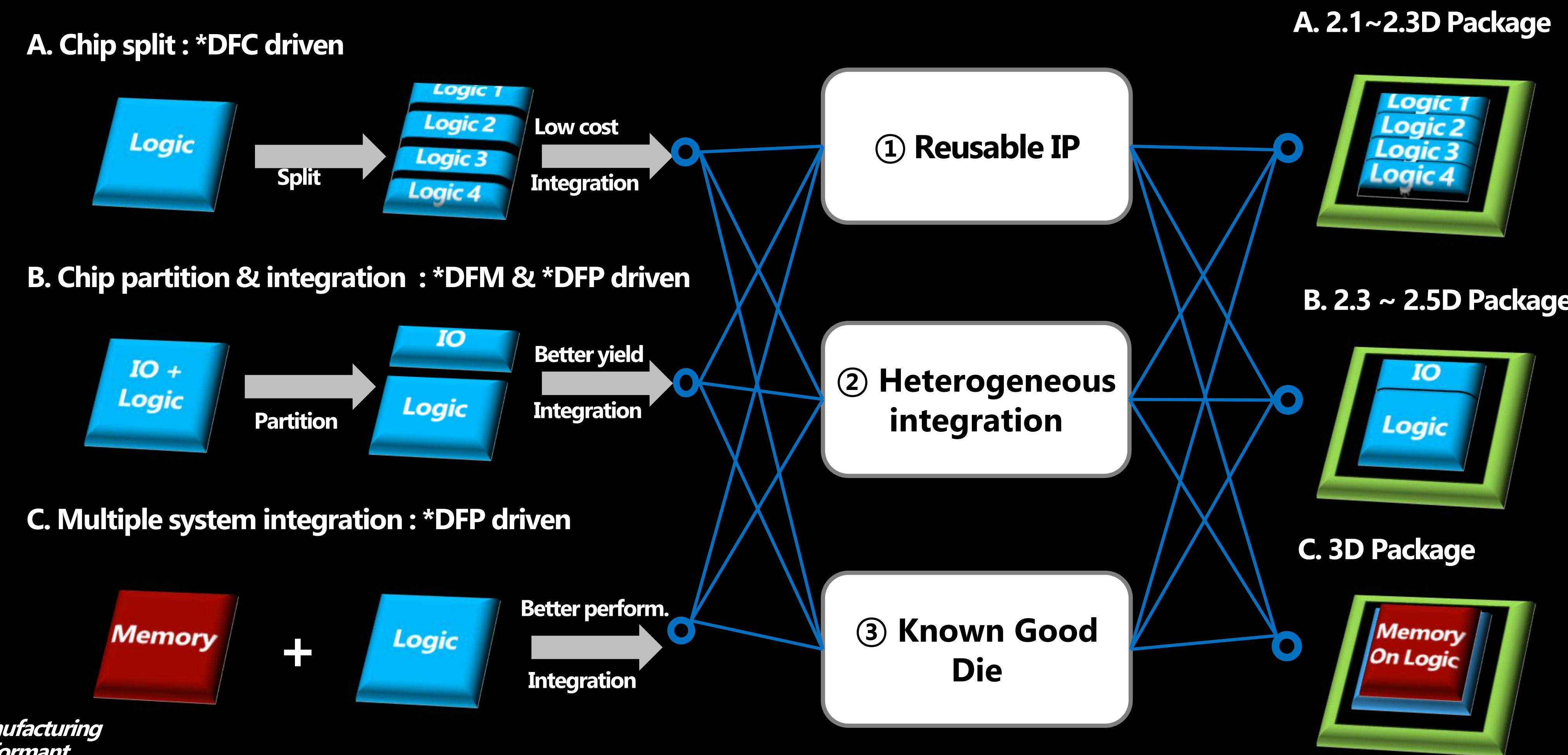
Die yield vs Chip area



From Behind the Yield: Exploring D_0 Challenges in TSMC × NVIDIA AI Chip Production

CoAsia Chiplet Solution (CoCs^{TM}) PKG Platform Introduction

- CoCs^{TM} is using 3kinds item to optimize Design For *C / M / P from SoC level



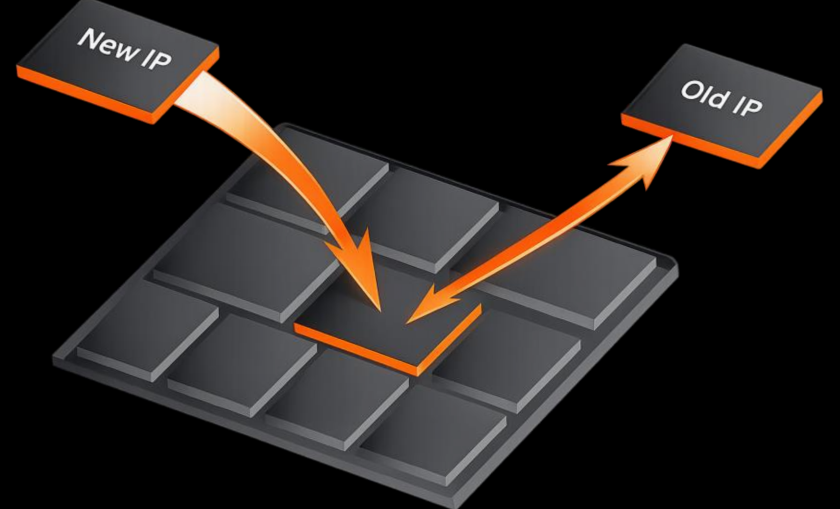
** Design For Manufacturing*
** Design For Performant*
** Design For Cost*

All-in-one Chiplet PKG Design & SCM Service

- CoCs™ can support All-in-one-service for PKG large scale and Hi-BW memory

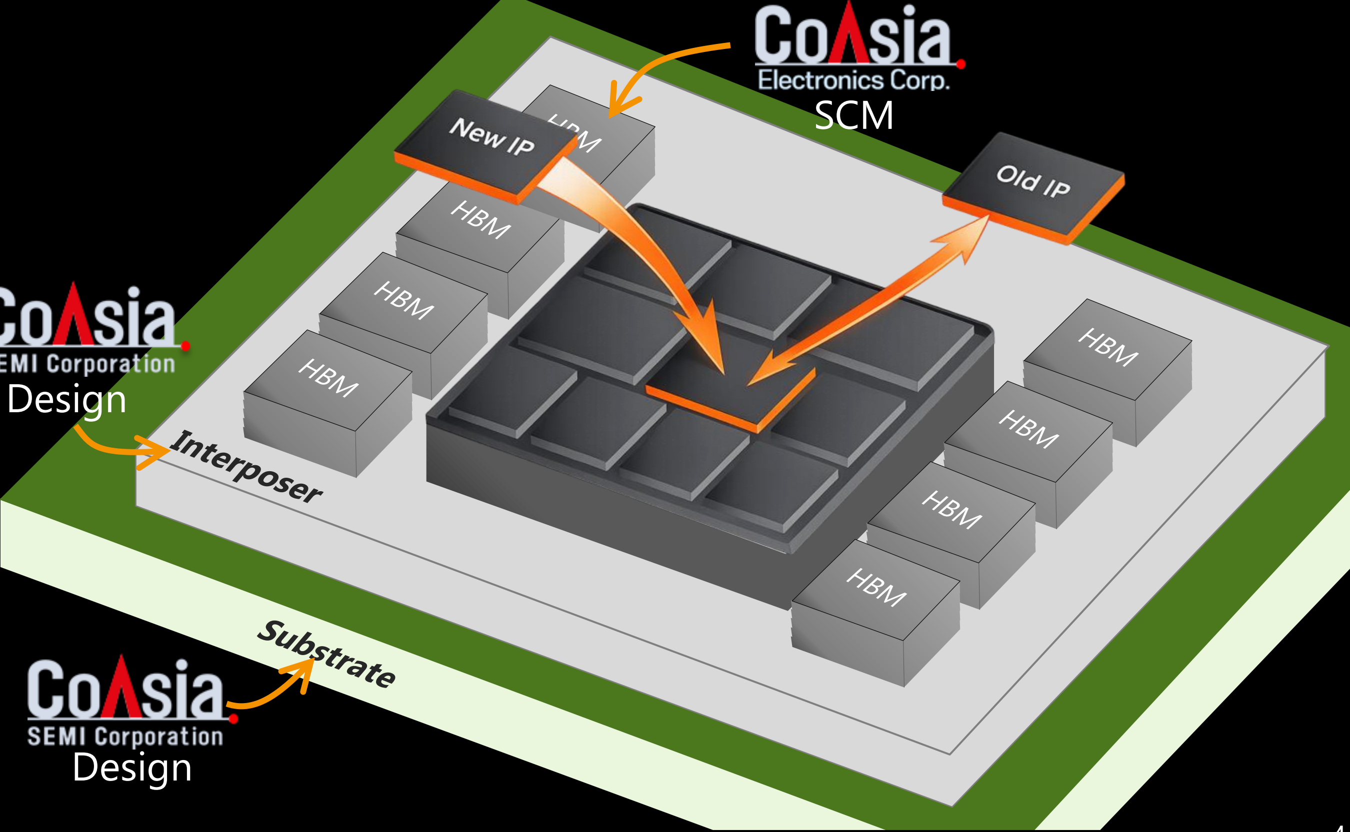
Customer wants to do

- Customized / Standardized IP is selected by PPAC
- Inference ↑ = IO count ↑ = bump count ↑ = PKG large scale
  = IO count ↑ = Bandwidth ↑ = Memory sourcing



CoAsia can support

- PKG platform can support w/ large scale + Hi-BW memory



CoCs™ PKG guide line

- CoCs™ can support PKG large scale and Hi-BW memory per geopolitical env.

Platform start

BIS and BW scale

Meet BIS spec.
- Yes → High band width?
  - Yes → 2.XD PKG
  - No → 2D PKG
- No → High band width?
  - Yes → 3D PKG
  - No → 2D PKG

PKG platform

2.XD PKG
- BW 4TBps: 4NPU+4HBM
- BW 8TBps: 8NPU+8HBM

2D PKG
- BW 1.2TBps: 4NPU+8DDR
- BW 2.4TBps: 8NPU+16DDR

3D PKG
- BW 35TBps: 1NPU ≒ 1 x reticle
- BW 10TBps: 1NPU ≒ 0.5 x reticle

HBM NPU NPU HBM
HBM NPU NPU HBM

Silicon interposer

RDL interposer

DDR NPU NPU DDR

3D MEM 4Hi
NPU

CoCs™ PKG Biz record

- CoCs™ has set up @ '23y and developed ~2.5D / 3D Advanced PKG

NPU / NPU / HBM | 3D DRAM | RDL Interposer | Silicon Interposer

Structure	2.5D 50body	2.3D 50body	2.5D 80body	2.3D 50body	3D 50body
Biz model	Si interposer design	RDL interposer + PKG design	Si interposer + PKG design / develop	RDL interposer + PKG design / develop	BE NPU design + PKG design / develop
E/S	'23y	'24y	'26y	'27y	'27y
Interposer type	Si ≤ 1x reticle	RDL ≤ 1x reticle	Si ≤ 3.5x reticle	RDL ≤ 1.2x reticle	NPU 1x reticle w/ TSV last
Si node	α nm	α nm	α nm	α nm	α + 4 nm
HSIF	UCIe / PCIe	UCIe / PCIe	UCIe / PCIe / ETH	BoW / PCIe / ETH	UCIe / PCIe
Memory	HBM2E	HBM3	HBM3E	GDDR7 (M/B)	3D customized DRAM
Adv. PKG top view	NPU HBM HBM	NPU HBM NPU	Confidential	Confidential	3D MEM 4Hi NPU

CoCs™ PKG platform road map

T.B.D

SoC Foundry		2026	2027	2028	2029	2030
Tech node		β nm		γ nm	δ nm	
IP	LPDDR, DDR	LPDDR Ref. A Gbps	LPDDR N-Gen. Ax1.3 Gbps		LPDDR N-N-Gen. Ax1.5 Gbps	
		DDR Ref. B Gbps		DDR N-Gen. Bx1.1 Gbps	DDR N-N-Gen.	
	MIPI	MPHY Ref. C Gbps	MPHY N-Gen. Cx2.0 Gbps		MPHY N-N-Gen.	
	SerDes	PCIe Gen. Ref. D Gbps	PCIe N-Gen. Dx2.0 Gbps		PCIe N-N-Gen.	
		Ethernet Ref. E Gbps	Ethernet N-Gen. Ex2.0 Gbps		Ethernet N-N-Gen. Ex4.0 Gbps	
	UCIe	UCIe-A Ref. F Gbps	UCIe-A N-Gen. Fx2.0 Gbps		UCIe N-N-Gen. Fx4.0 Gbps	
		UCIe-S Ref. F Gbps		UCIe-S N-Gen. Fx2.0 Gbps		
HBM	Generation	HBM Ref.	HBM N-Gen.			HBM N-N-Gen
	Stack density	Ref. G GB	Gx1.5 GB	Gx2.0 GB		~Gx3.0 GB
	Data rate	Ref. H Gbs		~Hx1.5 Gbps		~TBD Gbps
	I/O interface	HBM Ref. IO counts	IOx2.0 counts			TBD I/O
CoCs™ Platform		① ~2.5D, 8HBM, 5x Reticle Interposer	① 3D, 1x reticle	② ~2.5D + 3D, 12HBM, 8x Reticle Interposer		③ Quilt PKGing platform

CoCs™ PKG platform ecosystem

- **CoCs™ has set up partner ship for variable PKG platform**

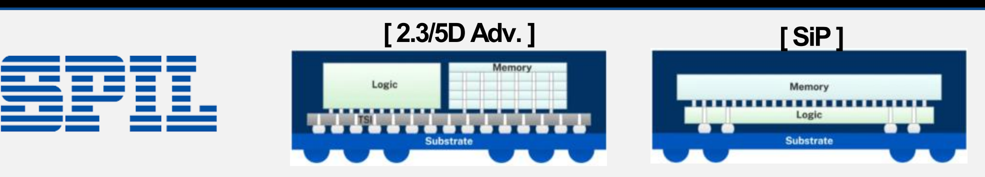
1st priority

[Quotation from Amkor]

[2.3/5D Adv.] [SiP]

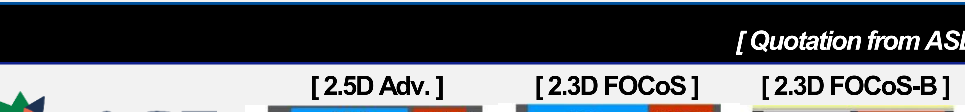
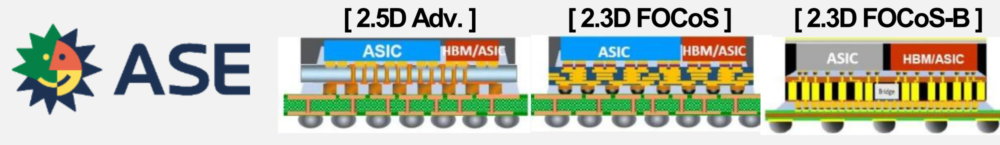
- **2.3/5D Advanced Package**
  - Several dies placed side by side above a variable interposer
- **System in Package**
  - Several dies placed side by side with thermal lid

[Quotation from SPIL]



- **2.3/5D Advanced Package**
  - Several dies placed side by side above a variable interposer
- **3D Advanced Package**
  - Smaller form factor in a single package for high BW & function

[Quotation from ASE]

- **2.5D Advanced Package**
  - Several dies placed side by side above a silicon interposer
- **FOCos line up**
  - Several dies on Fan Out Chip-on-Substrate w/ RDL interposer

[Quotation from IFS]

- **EMIB 2.5D**
  - Embedded Multi-die Interconnect Bridge 2.5D with TSVs
- **Foveros-R 2.5D**
  - Several dies placed side by side above a RDL interposer

CoCs™ PKG platform's EDA solution

- For successful history, Ansys + Huwin are strategic EDA in simulation war
- ① ~ ④ are showing how to meet more faster / exact by EDA

① HBM or another memory? ← Ansys + Huwin

③ UCIe or BoW? ← Ansys + Huwin

② PDN criteria? → Ansys

③ UCIe or BoW? → Ansys + Huwin

④ PCIe or Ethernet? → Ansys + Huwin

⑤ Thermal criteria? → Ansys

⑥ Warpage criteria? → Ansys

⑦ Low cost or high yield? What kind of interposer?

⑧ Low DK / DF / CTE?

High Speed InterFace simulation methodology

- Ansys HFSS is preferred to find the balanced between accuracy & server core

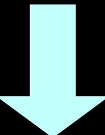
① HBM modeling (Interposer)

② Ethernet modeling (Interposer + Substrate)

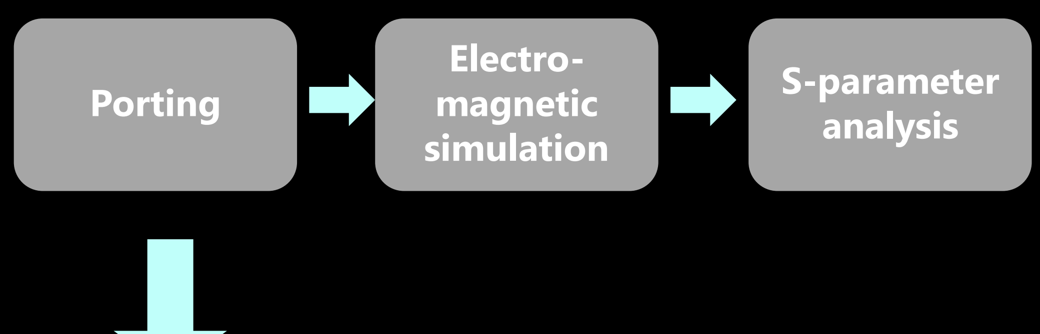
High Speed InterFace simulation methodology

- Ansys + Huwin is suggested combination to simulate Large IO count Chiplet PKG

③ Each modeling

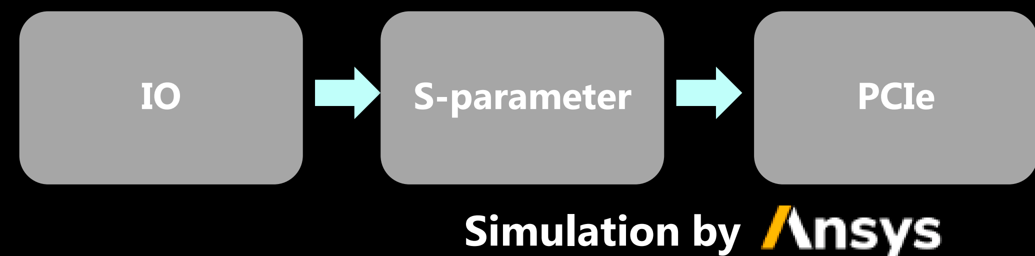


④ S-parameter simulation



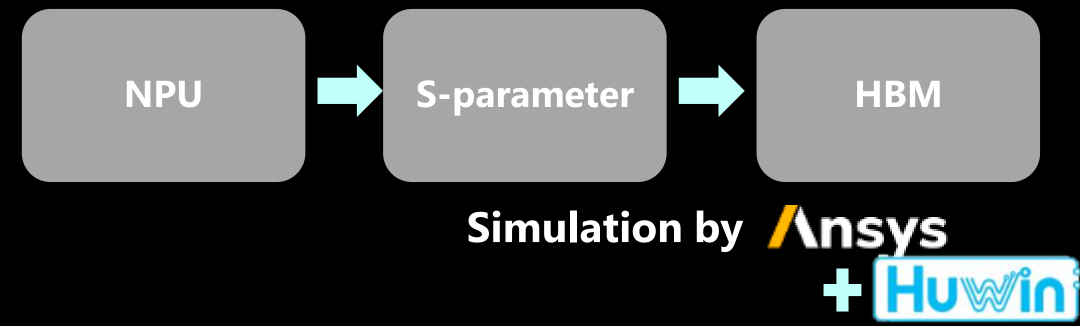
⑤ Touchstone export

⑥ Ethernet Channel Signal Integrity Simulation



Simulation by Ansys

⑦ HBM Channel Signal Integrity Simulation



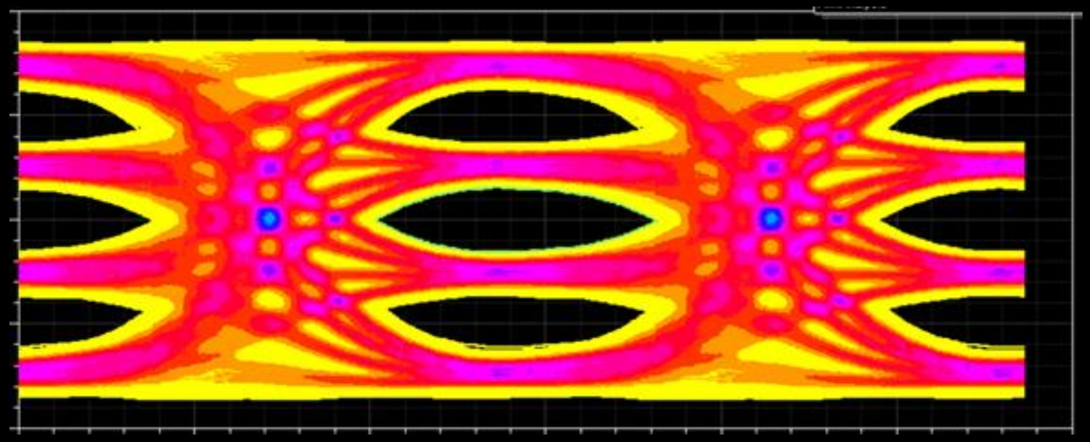
High Speed InterFace simulation methodology

- Ansys + Huwin is strong EDA to analyze Signal Integrity for Chiplet PKG

------Ethernet HSIF result ------

- Channel Circuit simulation @ Ansys

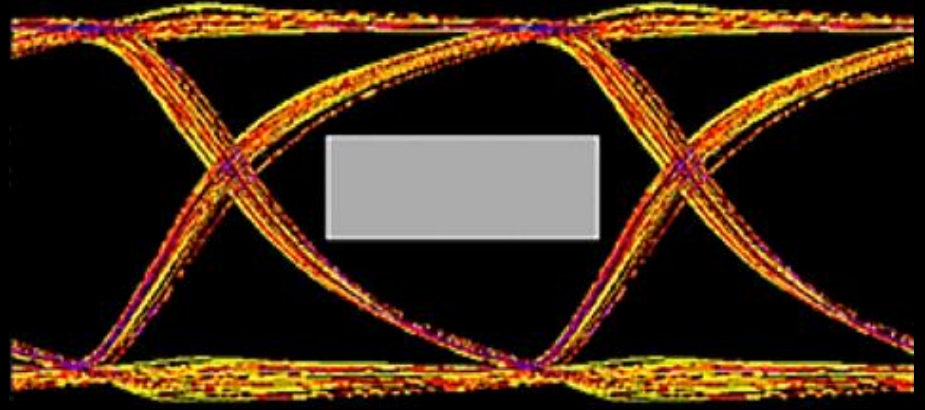
- Channel simulation result : Pass



--------HBM HSIF result--------

- Channel Circuit simulation @ Huwin ACVS

- Channel simulation result : Pass



Different points for Ansys+Huwin EDA

- Ansys + Huwin can support to be Winner at simulation war stage

Ansys + Huwin

3rd party EDA

25.6% Faster!

Same result!

Design, Source, Production

Our DSP, Your DSP

Thank You